WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

forming a removable gate over a substrate with a gate dielectric layer therebetween;

forming a dielectric layer over the substrate and exposing an upper surface of the removable gate;

removing the removable gate leaving an opening in the dielectric layer;

depositing a layer of tantalum (Ta) lining the opening;

heating in an oxidizing atmosphere to convert the Ta layer into a high-k gate dielectric layer; and

depositing a metal to fill the opening.

2. The method according to claim 1, comprising depositing the Ta layer by physical vapor deposition (PVD).

3. The method according to claim 2, comprising depositing the Ta layer at a thickness of 25 Å to 60 Å.

4. The method according claim 1, comprising heating in an atmosphere of flowing oxygen or flowing ozone to form a high-k tantalum oxide gate dielectric layer.

5. The method according to claim 4, comprising depositing the Ta layer by physical vapor deposition (PVD).

6. The method according to claim 5, comprising depositing the Ta layer at a thickness of 25 Å to 60 Å.

7. The method according to claim 1, comprising heating in an atmosphere of flowing oxygen and N_2O or flowing ozone and N_2O to form a high-k tantalum oxynitride gate dielectric layer.

8. The method according to claim 7, comprising depositing the Ta layer by physical vapor deposition (PVD).

9. The method according to claim 8, comprising depositing the Ta layer at a thickness of 25 Å to 60 Å.

10. The method according to claim 1, comprising heating the Ta layer in an oxygen or ozone plasma to form a high-k tantalum oxide gate dielectric layer.

11. The method according to claim 10, comprising depositing the Ta layer by physical vapor deposition (PVD).

12. The method according to claim 11, comprising depositing the Ta layer at a thickness of 25 Å to 60 Å.

13. The method according to claim 1, comprising heating in a plasma containing oxygen and N_2O or ozone and N_2O to form a high-k tantalum oxynitride gate dielectric layer.

14. The method according to claim 13, comprising depositing the Ta layer by physical vapor deposition (PVD).

15. The method according to claim 14, comprising depositing the Ta layer at a thickness of 25 Å to 60 Å.

16. The method according to claim 1, comprising planarizing by chemical mechanical polishing (CMP) such that an upper surface of the metal filling the opening is substantially coplanar with an upper surface of the dielectric layer.

17. The method according to claim 1, comprising annealing in a plasma containing ammonia after oxidizing to form the high-k dielectric layer.

18. The method according to claim 1, comprising removing the gate dielectric layer before depositing the Ta layer.